REMARKS

Claims 1-60 are pending. Claims 1-6, 8-9, 16-17, 19-22, 24-25, 29, 31-33, 35-36, 40, 42-47, 57-58, and 60 were rejected under 35 USC 102(e) as being anticipated by Aung, et. al., Pub. No. US 2001/0033188 A1 (hereinafter referred to as Aung). Claims 7, 10-15, 18, 23, 26-28, 30, 34, 37-39, 41, 48-56, and 59 were objected to as being dependent upon a rejected base claim. The Applicants respectfully traverse the above rejections and objections.

Amended Claim 1 includes, among other features, a down-level shifter connected to the dedicated routing structure. This is supported by down-level shifter 341 in Figure 3 and paragraph 24 of the specification. Aung neither discloses nor suggests a down-level shifter, hence claim 1 should be allowable.

Claims 2-19 being dependent upon claim 1 should be allowable for at least the same reason claim 1 is allowable.

Amended Claim 20 includes the limitations of claim 26 and should now be allowable.

Claims 21-23, and 27-30 being dependent upon claim 20 should be allowable for at least the same reason claim 20 is allowable.

Claims 24-26 have been deleted as they are no longer dependent claims of the amended claim 20.

Amended Claim 31 includes the limitations of claim 37 and should now be allowable.

Claims 32-34, and 38-41 being dependent upon claim 31 should be allowable for at least the same reason claim 31 is allowable.

Claims 35-37 have been deleted as they are no longer dependent claims of the amended claim 31.

Amended Claim 42 includes the limitations of claim 48. Aung neither discloses nor suggests, a second logic gate having input terminals coupled to receive a clock signal on the second clock trace and the inverse of the select signal, and an output

terminal coupled to the second transmission gate. Hence claim 42 should be allowable.

Claims 43-47, and 49-60 being dependent upon claim 42 should be allowable for at least the same reasons claim 42 is allowable.

New Claim 61 includes, among other features, selectively routing on dedicated routing resources either the first clock signal from the first pair of clock pads or the second clock signal from the second pair of clock pads to a phase locked loop of a multi-gigabit transceiver located on the programmable logic device. This is supported by Figure 3 and paragraphs 24-34 of the specification, where, for example, REF_CLK_2.5V 211 or REF_CLK_1.5V 213 is selectively routed via MUX 313 to TX PLL 351.

Aung, as seen by FIG. 10 and the Examiner's comments on claims 1 and 3 (pages 2-3 of the Office Action), has a first pair of clock pads (pads connected to buffer 42a) connected to a first PLL 100a and a second pair of clock pads (pads connected to buffer 42b) connected to a second PLL 100b. Hence Aung neither discloses nor suggests the above stated feature of Claim 61.

New Claims 62-65 being dependent upon claim 61 should be allowable for at least the same reasons claim 61 is allowable.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on September 11, 2003.

Pat Slaback
Name

Signature